WHAT IS CLAIMED IS:

1. An output control circuit, which is used together with transfer means in which a number of unit circuits that shift a starting pulse sequentially in synchronization with a clock signal are in cascade connection with each other, and generates a set of a positive logic output signal and a negative logic output signal which is an inversion of the positive logic output signal based on an output signal from each of the unit circuits, the output control circuit having,

a first logic operation unit which, based on an output signal from a unit circuit and an output signal from a subsequent-stage unit circuit, generates an output signal that is enabled in a period while the output signals from the two unit circuits are enabled at the same time, and,

a second logic operation unit which generates the positive logic output signal and the negative logic output signal based on the output signal from the first logic operation unit, and controls an enabling period of the positive logic output signal or the negative logic output signal based on the output signal from a first logic operation unit in a subsequent-stage output control circuit.

2. The output control circuit according to claim 1 characterized in that the second logic operation unit has a first system that generates the positive logic output signal based on the output signal from the first logic operation unit, and a second system that generates the negative logic output signal based on the output signal from the first logic operation unit, wherein one of a system, the first system or the second system, having a longer delay time has a logic circuit that controls an enabling period of the positive logic output signal or the negative logic output signal which should be generated in one of the system based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

3. The output control circuit according to claim 2 characterized in that the output signal from the first logic operation unit is enabled at low level,

and the logic circuit in the second logic operation unit is a NAND circuit that is included in the second system, and controls the enabling period of the negative logic output signal based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

4. The output control circuit according to claim 3 characterized in that the output signal from the unit circuit is enabled at high level,

the first logic operation unit has a NAND circuit,

the first system in the second logic operation unit has a first inverting circuit that inverts an output signal from the NAND circuit in the first logic operation unit and then outputs the signal as the positive logic output signal,

the second system in the second logic operation unit has a second inverting circuit that inverts the output signal from the NAND circuit in the first logic operation unit and then outputs the signal, and the logic circuit that operates inversion of a logical product of the output signal from the second inverting circuit and the output signal from the first logic operation unit in the subsequent-stage output control circuit and then outputs the inversion of the logical product as the negative logic output signal.

5. The output control circuit according to claim 2 characterized in that the output signal from the first logic operation unit is enabled at high level,
and the logic circuit in the second logic operation unit is a NOR circuit that is included in the first system, and controls the enabling period of the positive logic output signal based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

6. The output control circuit according to claim 5 characterized in that the output signal from the unit circuit is enabled at low level,

the first logic operation unit has a NOR circuit,

the second system in the second logic operation unit has a first inverting circuit that inverts an output signal from the NOR circuit in the first logic operation unit and then outputs the signal as the negative logic output signal, and

the first system in the second logic operation unit has a second inverting circuit that inverts the output signal from the NOR circuit in the first logic operation unit and then outputs the signal, and the logic circuit that operates the inversion of the logical sum of the output signal form the second inverting circuit and the output signal from the first logic operation unit in the subsequent-stage output control circuit and then outputs the inversion of the logical sum as the positive logic output signal.

7. The output control circuit according to claim 2 characterized by having a level conversion circuit that converts amplitude of signal in a previous stage of the logic circuit.

8. The output control circuit according to claim 7 characterized in that the output signal from the unit circuit is enabled at high level,

the first logic operation unit has the NAND circuit, and

the second logic operation unit has the second inverting circuit that inverts the output signal from the NAND circuit in the first logic operation unit,

the level conversion circuit that converts an amplitude of each signal of the output signal from the NAND circuit in the first logic operation unit and the output signal from the second inverting circuit and then outputs the signal,

a first inverting circuit that inverts the output signal, which is level converted, from the NAND circuit in the first logic operation unit, and then outputs the signal as the positive logic output signal, and

the logic circuit that operates the inversion of the logical product of the output signal, which is level converted, from the second inversion circuit, and the output signal, which is level converted in the subsequent-stage output control circuit, from the first logic operation unit, and then outputs the inversion of the logical product as the negative logic output signal.

9. The output control circuit according to claim 7 characterized in that the output signal from the unit circuit is enabled at low level,

the first logic operation unit has the NOR circuit, and

the second logic operation unit has a second inverting circuit that inverts the output signal from the NOR circuit in the first logic operation unit,

the level conversion circuit that converts the amplitude of each signal of the output signal from the NOR circuit in the first logic operation unit and the output signal form the second inverting circuit and then outputs the signal,

a first inverting circuit that inverts the output signal, which is level converted, from the NOR circuit in the first logic operation unit, and then outputs the signal as the negative logic output signal, and

the logic circuit that operates the inversion of the logical sum of the output signal, which is level converted, from the second inverting circuit, and the output signal, which is level converted in the subsequent-stage output control circuit, from the first logic operation unit, and then outputs the inversion of the logical sum as the positive logic output signal.

10. The output control circuit according to claim 1 characterized by having an electric current amplification unit that is provided in a later stage of the second logic operation unit and performs an electric current amplification for respective output signals from the second logic operation unit and then outputs the signals as the positive logic output signal and the negative logic output signal.

11. The output control circuit according to claim 1 characterized by having a holding unit provided in a later stage of the second logic operation unit for holding respective

output signals from the second logic operation unit bi-directionally, wherein respective signals from the holding unit are output as the positive logic output signal and the negative logic output signal.

12. A driving circuit, which drives an electro-optic apparatus having a number of scan lines, a number of data lines, pixel electrodes and switching elements arranged in a matrix pattern corresponding to intersections of the scan lines and the data lines, the driving circuit characterized by having,

a transfer means in which unit circuits that shifts a starting pulse sequentially in synchronization with a clock signal are in a cascade connection with each other, and

an output control means having a number of the output control circuits according to claim 1.

13. An electro-optic apparatus characterized by having,

a number of the scan lines,

a number of the data lines,

the pixel electrodes and the switching elements arranged in a matrix pattern corresponding to the intersections of the scan lines and the data lines,

a image signal line through which an image signal is supplied,

a number of switching circuits provided corresponding to each of the data lines, in which an on/off control is performed by a set of a control signal that is enabled at high level and a control signal that is enabled at low level, and one terminal is connected to the data line and the other terminal is connected to the image signal line, and

the driving circuit according to claim 12, which supplies the positive logic output signal and the negative logic output signal to each of the switching circuits as the set of the control signals.

14. An electronic instrument characterized by having the electro-optic apparatus according to claim 13.